- 1 DESCRIPTION

CERAMIC CIRCUIT BOARD, METHOD FOR PRODUCING THE SAME, AND POWER MODULE

Technical Field

The present invention relates to a ceramic circuit board, which is a joined body (bonded body) of a ceramic member and a metal circuit layer, a method for producing the same, and a power module including the ceramic circuit board. In particular, the present invention relates to a ceramic circuit board in which the generation of voids in the joint interface can be effectively suppressed, the joint strength (bonding strength) of the metal member serving as the circuit layer can be increased, and the heat resistance cycle characteristics can be drastically improved, a method for producing the same, and a power module.

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Background Art

Hitherto, as a method for joining (bonding) a ceramic member and a metal circuit member, a simultaneous sintering method (co-fire method) of printing paste of a high melting point metal (refractory metal) such as Mo or W on the surface of a ceramic sheet-shaped molding and then sintering, a DBC method (direct bonding copper method) in which a circuit layer is integrally joined on the surface of a ceramic substrate using a eutectic reaction between copper serving as a circuit material and oxygen, an active metal brazing method using a brazing material containing an active metal such as Ti as a joining material of a metal circuit layer, and the like have been widely used.

Joined bodies of a ceramic member and a metal member produced by the

above-described joining methods are used in various fields. A typical example thereof is a ceramic circuit board for mounting and joining a semiconductor device and the like. Examples of characteristics required for such a ceramic circuit board include satisfactory heat dissipation effect (heat radiating property), high structural strength as a whole ceramic circuit board, high joint strength (bonding strength) between a ceramic substrate and a metal circuit plate, and satisfactory heat resistance cycle characteristics as a circuit board.

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As a ceramic substrate constituting the ceramic circuit board, a sintered body of aluminum nitride (AlN), aluminum oxide (Al₂O₃), or silicon nitride (Si₃N₄) has been widely used.

For example, an aluminum nitride substrate is particularly excellent in heat dissipation effect because it has a high thermal conductivity of 160 W/m·K or more, which is higher than that of other ceramic substrates. A silicon nitride substrate has a three-point bending strength (at room temperature) of 600 MPa or more, and thus the strength of the circuit board can be improved when silicon nitride is used as a material for a ceramic substrate. In contrast, an aluminum oxide substrate has a thermal conductivity of about 20 W/m·K and a three-point bending strength of about 360 MPa. Therefore, in particular, in order to achieve high heat dissipation effect and high structural strength, use of a nitride ceramic substrate is more preferable for a circuit board, compared with an oxide ceramic substrate.

In view of the joint strength between a ceramic substrate and a metal circuit plate, among the above-described joining methods, the active metal brazing method is preferred. In the active metal brazing method, a metal foil containing at least one active metal such as Ti, Hf, Zr, and Nb or paste prepared by adding these active metals to an Ag-Cu brazing material is applied between the ceramic substrate and the metal circuit plate, and both members are then integrally joined and bonded by

heat treatment. When a joining by the active metal brazing method is performed using a nitride ceramic substrate, a joint layer composed of a nitride of the above active metal is formed after the heat treatment, resulting in the formation of a stronger joint state. Thus, a joined body of a nitride ceramic and a metal member prepared by the active metal brazing method satisfies the characteristics required for a circuit board. Accordingly, such a joined body has been widely used as a substrate for electronic circuits, such as a substrate for a semiconductor module (power module) on which a power semiconductor device is mounted.

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In addition, as a known insulating circuit board for mounting a semiconductor, the following circuit board has also been proposed: The circuit board has a structure in which, for example, a metal circuit layer is laminated and bonded on at least one of the surfaces of a ceramic substrate with an Al-Si- or Al-Ge-based brazing material for the metal layer therebetween. By adjusting the Vickers hardness and the thickness of the metal layer and the thickness and the flexural strength of the ceramic substrate to predetermined values, the heat resistance cycle life of the circuit board is extended (see, for example, Patent Document 1).

Furthermore, as a known ceramics wiring board, a wiring board prepared by forming a metal layer such as an Al or Ni layer that has excellent wettability with a brazing material and that has a thickness of 1 to 10 µm on the surface of a ceramic substrate has also been proposed (see, for example, Patent Document 2).

[Patent Document 1] Japanese Unexamined Patent Application Publication No. 2001-144234

[Patent Document 2] Japanese Unexamined Patent Application Publication No. 2002-111211

However, in the above known circuit boards, although the structural strength is improved to some degree, the heat resistance cycle characteristics do not

necessarily satisfy the present technical requirement. The reason for this is as follows: As the capacity, the output, and the integration degree of recent semiconductor devices increase, the heat generating amount from the devices tends to increase. When the heating value increases, cracks due to the difference in thermal expansion between the metal circuit plate and the ceramic substrate are easily generated in the ceramic substrate and the brazing material layer, resulting in problems such as a decrease in the withstand voltage of the ceramic substrate and separation of the metal circuit layer. In particular, when the metal circuit layer is joined by the active metal brazing method, a phase of a nitride of the active metal is formed on the surface adjacent to the nitride ceramic. Although this active metal nitride phase effectively acts on the improvement of the joint strength, the phase does not have a function for releasing a stress generated by the difference in thermal expansion. Consequently, cracks are easily generated in the ceramic substrate, resulting in the problem of degrading the durability of the circuit board.

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In order to solve the above-described problem, a method is also employed in which, instead of the copper plate serving as the circuit layer, an aluminum plate is used and is joined with a ceramic substrate with an Al alloy brazing material therebetween. The aluminum has not only a conductivity next to that of copper and high heat dissipation effect but also a property that plastic deformation is easily caused by a thermal stress. Therefore, the generation of cracks in the ceramic substrate, solder, and the like can be prevented.

On the other hand, an Al-Si alloy forms a joint by bonding to oxygen that is present on the surface of the ceramic substrate. However, unlike a substrate made of an oxide ceramic represented by alumina, particularly in a substrate made of a nitride ceramic such as aluminum nitride or silicon nitride, since the oxygen content per unit area of the substrate structure is low, the bondability (i.e., wettability of the

interface between the Al-Si alloy and the ceramic) is low. In order to compensate for this disadvantage, the joining is performed while a load is applied. However, because of a problem relating to the bondability with aluminum nitride, and in particular, silicon nitride, the heat resistance cycle characteristics are varied. Thus, the countermeasure is not sufficient.

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As described above, in order to improve the wettability of the brazing material, a method of forming an AI metal film on the surface of a ceramic substrate and then joining the substrate is also employed. However, a phenomenon in which the surface of the structure partly rises because of the diffusion of AI elements in the AI metal film, i.e., the hillock phenomenon, occurs. Consequently, voids (air gaps) are easily formed between the AI metal film and the AI-Si brazing material, resulting in a decrease in the joint strength of the metal circuit layer. Thus, disadvantageously, the heat resistance cycle characteristics as the whole circuit board is easily degraded. Furthermore, since the AI metal film is formed so that the thickness of the film is as large as about 1 to 10 μ m, the time required for vapor deposition of AI metal is increased, resulting in the problem of an increase in the production cost.

In the semiconductor field, in addition to the developments of integration degree and the increase in the operation speed of LSIs, for example, the applications of power devices such as GTO and IGBT (insulated gate bipolar transistor) have been increasing. Under this situation, the heating value (amount of heat) generated from a silicon chip (semiconductor element) has been steadily increasing. When the power modules are used in the fields requiring a long-term reliability, such as electric railroad vehicles and electric automobiles, the heat dissipation effect and the durability of a circuit board having a silicon chip thereon or a module including the circuit board therein are of more concern. Unfortunately, in the known power modules, the durability of the joined part is insufficient and satisfactory reliability

cannot be ensured.

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The present invention has been made in order to solve the above-mentioned problems in the related art. In particular, it is an object of the present invention to provide a ceramic circuit board in which the generation of voids in the joint interface can be effectively suppressed, the joint strength of a metal member serving as a circuit layer can be increased, and the heat resistance cycle characteristics can be drastically improved, a method for producing the same, and a power module including the circuit board.

10 Disclosure of Invention

In order to achieve the above object, the present inventors have conducted various studies of a method for effectively preventing or suppressing the diffusion of Al elements that causes the hillock phenomenon. As a result, the present inventors have found the following knowledge: In particular, instead of the conventional Al metal film, by forming an Al alloy film having a predetermined thickness on the surface of a ceramic substrate, even when the thickness of the Al alloy film is small less than 1 μ m, the hillock phenomenon can be satisfactorily suppressed, the generation of voids in the joint surface can be effectively prevented, and the joint assembly of the circuit board can be simplified to reduce the production cost drastically. This finding and knowledge resulted in completion of the present invention.

Namely, according to a ceramic circuit board of the present invention, in a ceramic circuit board prepared by integrally joining a circuit layer composed of a clad member including an Al plate and an Al-Si brazing material to a ceramic substrate, a surface of the clad member adjacent to the Al-Si brazing material is joined to the ceramic substrate with an Al alloy film therebetween, the Al alloy film having a

thickness of less than 1 μm and being provided on the surface of the ceramic substrate.

In the present invention, the circuit layer is composed of a clad member including an Al plate and an Al-Si brazing material. In view of the current-carrying capacity, the thickness of the circuit layer is preferably set to the range of 0.15 to 0.5 mm.

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In the ceramic circuit board, the ceramic substrate is preferably composed of an aluminum nitride sintered body or a silicon nitride sintered body.

The ceramic substrate constituting the ceramic circuit board of the present invention is not particularly limited as long as the ceramic substrate has a predetermined heat dissipation effect and structural strength. Substrates composed of a sintered body of a nitride ceramic such as aluminum nitride, silicon nitride, or sialon (Si-Al-O-N); a sintered body of a carbide ceramic such as silicon carbide (SiC); and a sintered body of an oxide ceramic such as aluminum oxide (Al₂O₃) or zirconia (ZrO₂) can be suitably used. However, high effect of improving the bondability (bonding property) can be achieved even in the nitride ceramic substrates, which have a low oxygen concentration on the surface of the substrate structure. Accordingly, when the ceramic substrate is an aluminum nitride substrate or a silicon nitride substrate, particularly excellent operation and effect can be obtained.

The Al alloy film disposed on the surface of the ceramic substrate improves the wettability of the Al-Si brazing material and increases the joint strength of the clad member serving as the circuit layer bonded to the ceramic substrate. The Al alloy film is formed by sputtering method, vapor deposition method, or the like. Furthermore, according to such an Al alloy film, the diffusion and the migration of Al elements do not occur during joining by heating, and voids due to the Al diffusion are not generated. The thickness of the Al alloy film is less than 1 μm. When the

thickness of the AI alloy film is excessively small to be less than 0.1 μ m, the above improvement effect of the wettability is not sufficient. On the other hand, when the AI alloy film is formed so as to have a thickness of 1 μ m or more, the above effect is saturated and it takes a long time to form the AI alloy film, resulting in a decrease in production efficiency. Accordingly, the thickness of the AI alloy film is set to less than 1 μ m, but is more preferably set to the range of 0.1 to 0.5 μ m.

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In the above ceramic circuit board, the Al alloy film preferably contains at least one rare earth element selected from Y, Sc, La, Ce, Nd, Sm, Gd, Tb, Dy, Er, Th, and Sr in an amount of 1 to 5 atomic percent. When the Al alloy film is formed using an alloy containing the predetermined rare earth element in the predetermined content, in particular, the wettability of the brazing material can be adjusted more appropriately, the loss by flowing of the brazing material due to the excessive increase in the wettability can be prevented, the joint strength of the circuit layer can be further increased, and the generation of voids in the joint surface can be effectively prevented.

Furthermore, in the above ceramic circuit board, the Al content of the Al-Si brazing material is preferably 85 mass percent or more and the Si content thereof is preferably in the range of 6 to 15 mass percent. When the Al content and the Si content of the Al-Si brazing material are in the above ranges, the brazing material has a melting point lower than that of Al by 50°C to 100°C. Consequently, the joining of an Al-Si alloy layer serving as the circuit layer is simply performed and the joining with the Al-Si brazing material is also easily performed.

According to a method for producing the above-described ceramic circuit board of the present invention, in a method for producing a ceramic circuit board prepared by integrally joining a circuit layer composed of a clad member including an Al plate and an Al-Si brazing material to an Al alloy film, the circuit layer composed of

the clad member including the Al plate and the Al-Si brazing material and a ceramic substrate having the Al alloy film thereon overlap with each other, and the circuit layer and the ceramic substrate are then joined by heating at a temperature of 580°C to 630°C in an atmosphere of a degree of vacuum of 10⁻² Pa or lower while a pressing load is applied so that the pressure is 0.2 MPa or more.

In the above production method, when the pressure during joining is less than 0.2 MPa, the adhesiveness between the circuit layer composed of the clad member and the ceramic substrate becomes insufficient. Furthermore, in an atmosphere where the degree of vacuum is in the above range, oxidation of Al-Si proceeds and the wettability is increased to improve the bondability. Furthermore, by heating in the above joint temperature range (580°C to 630°C), the circuit layer composed of the clad member can be integrally joined to the ceramic substrate having an Al alloy film thereon in a short period of time.

A power module according to the present invention includes a ceramic circuit board prepared by integrally joining a circuit layer composed of a clad member including an Al plate and an Al-Si brazing material to a ceramic substrate, wherein a surface of the clad member adjacent to the Al-Si brazing material is joined to the ceramic substrate with an Al alloy film therebetween, the Al alloy film having a thickness of less than 1 µm and being provided on the surface of the ceramic substrate; a semiconductor element mounted on the circuit layer; and a heat sink that dissipates heat generated from the semiconductor element via the ceramic circuit board.

Brief Description of the Drawings

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Fig. 1 is a cross-sectional view showing the structure of a ceramic circuit board according to an embodiment of the present invention.

Fig. 2 is a cross-sectional view showing an example of the structure of a power module including the ceramic circuit board according to the present invention.

Best Mode for Carrying Out the Invention

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Embodiments of a ceramic circuit board of the present invention will now be described specifically with reference to the attached drawings.

[Examples 1 to 116 and Comparative Examples 1 to 45]

As shown in Tables 1 to 6, as ceramic substrates used in examples and comparative examples, a large number of silicon nitride (Si_3N_4) substrates, aluminum nitride (AIN) substrates, sialon (Si-AI-O-N) substrates, silicon carbide (SiC) substrates, and aluminum oxide (AI_2O_3) substrates that have a thickness of 0.625 to 1.2 mm were prepared. A blasting process and a polishing process were performed on a surface of each ceramic substrate for joining a clad member serving as a circuit layer so that the surface roughness (Ra) was controlled to be 1 μ m.

Subsequently, an Al alloy film having the composition and the thickness that were shown in Tables 1 to 6 was formed by vapor deposition on a part of each ceramic substrate for joining the circuit layer, the ceramic substrate having an adjusted surface roughness.

On the other hand, an Al circuit plate and an Al-Si brazing material that had the compositions shown in Tables 1 to 6 were integrally joined so as to have a thickness ratio of 75:25 by rolling operation. Thus, clad members serving as the circuit layer were prepared. The thicknesses of the resulting clad members were determined to the values shown in Tables 1 to 6.

Subsequently, each of the circuit layers composed of the clad member including the Al plate serving as the circuit plate and the Al-Si brazing material and each of the ceramic substrates having an Al alloy film (Examples) or an Al metal film

(Comparative Example 1) thereon, which were prepared as described above, overlapped with each other. Each of the circuit layers and each of the ceramic substrates were then joined by heating to a temperature shown in Tables 1 to 6 in an atmosphere of a degree of vacuum shown in Tables 1 to 6 while a pressing load was applied so that the pressure was a value shown in Tables 1 to 6. Thereby, ceramic circuit boards of the examples and the comparative examples were produced.

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As shown in Fig. 1, a ceramic circuit board 1 produced as described above has a structure in which a circuit layer 4 composed of a clad member including a circuit plate 2 made of an Al plate and an Al-Si brazing material layer 3 is integrally joined on the surface of a ceramic substrate 6 having an Al alloy film 5 (Examples) or an Al metal film (Comparative Example 1) thereon.

In order to evaluate the characteristics of the ceramic circuit boards of the examples and the comparative examples produced as described above, the following measurement tests were performed. First, a void ratio on the joint surface disposed under the circuit layer of each ceramic circuit board was measured with an ultrasonic flaw detector. The void ratio was determined by analyzing an image of voids that are present on the joint surface of a 20 mm square, the image being taken by the ultrasonic flaw detector. The void ratio was measured as a void area ratio per 20 mm square of the jointed area.

A joint strength was measured as follows: The circuit layer 4 of the ceramic circuit board 1 of each example and each comparative example was pulled upward in the vertical direction in Fig. 1. The value calculated by dividing the tensile load when the circuit layer 4 was peeled and separated from the ceramic substrate 6 by the jointed area was defined as the joint strength. Tables 1 to 6 show the measured values, the specifications of the ceramic circuit boards, the joining conditions, and the like.

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QIOA	RATIO	(%)	6	5.6	2.3	. 0.3	7.8	8.9	4.3	3.1	7.5	2.8	0.7	4.5	2.4	1.4	0	0	2	0	9.0	5.5	0.2	0.4	1.6	2.2	9	0	3.6	0.2	3.3	1.5
JOINING	STRENGH	(N∕20mm□)	45	47.3	55.8	61.9	48.2	46.8	41.2	43.5	63.2	60.4	58.2	50.3	53.6	61.9	63.3	64.5	53.7	64.6	56.3	47.8	59.2	61.5	55.9	48.4	45.5	62.7	51.8	58.9	51.2	55.6
ENT	TEMPE- RATURE	(၁့)	009	580	009	290	630	620	009	610	610	009	620	009	630	290	280	280	580	280	580	909	605	605	610	600	605	900	615	620	620	615
JOINING TREATMENT	DEGREE OF VACUUM	(Pa)	10-2	10-2	10-2	10_5	10-2	10_5	10-2	10-2	10_5	10-2	10-2	10-2	10-2	10-2	10_5	10_5	10-5	10-2	10-2	10-2	10-2	10-5	10_5	10-2	10-2	10-2	10-2	10-2	10-2	10-2
NINIOC	PRESSING DEGREE OF LOAD VACUUM	(MPa)	0.2	1	0.3	9.0	1	8.0	0.5	0.5	0.3	0.3	1	0.5	0.2	1.5	1	2.5	0.5	2	1	0.5	2	1.5	0.5	0.2	1	2	1	1.5	0.2	0.5
SURFACE STRATE	THICKNESS	(m m)	0.5	0.1	8.0	0.5	0.2	0.1	0.3	0.5	0.3	0.4	0.3	1.0	9.0	0.5	0.1	9.0	0.1	8.0	9.0	0.5	0.5	0.3	0.3	9.0	0.1	0.5	0.3	0.5	0.2	0.1
AI ALLOY FILM ON SURFACE OF CERAMIC SUBSTRATE	COMPOSITION	(at%)	5Y—AI	4G4-AI	3Er-A!	4Y-1Ce-Al	ANA-AI	5Sc-Al	3Y-1La-05Sr-AI	3Dy-1Th-Al	3Tb-Al	3Y AI	3Y-A!	1Y-AI	3Nd-AI	3Er-AI	3Y-AI	3Y-AI	4Sm-Al	5Gd-Al	4Sc-Al	1Y-AI	1Er-Al	2Sr-Al	2Ce-Al	2Dy-Al	4Th-Al	3Y-AI	5Tb-Al	4La-Al	1Gd-Al	5Er-Al
(CIRCUIT LAYER)	TOTAL	(mm)	0.2	0.5	0.3	0.5	0.3	0.15	0.3	0.5	0.3	0.5	0.2	0.5	0.2	0.2	0.15	0.2	0.2	0.2	0.3	0.5	0.5	0.2	0.15	0.5	0.1	0.3	0.5	0.3	0.2	0.4
MEMBER	COMPOSITION OF AI-SI BRAZING	MATERIAL (MASS%)	15Si-Al	7.5Si-AI	10Si-Al	10Si-Al	10Si-AI	6Si-Al	8Si-Al	7.5Si-Al	10Si AI	7.5Si-Al	15Si-AI	15Si-AI	15Si-Al	15Si-Al	1,2Si-Al	12Si-Al	12Si-Al	12Si-Al	12Si-Al	10Si-Al	10SiAl	10SiAI	10Si-Al	10Si – Al	7.5Si — Al	7.5Si Al	7.5Si — Al	7.5Si-Al	7.5Si — Al	7.5Si-Al
STRUCTURE OF CLAD	AI CONTENT IN	(MASS%)	98AI	97AI	98AI	95AI	98AI	96AI	95AI	99AI	98AI	97AI	99AI	1966	97Ai	96AI	99AI	99AI	98AI	98AI	95AI	99AI	98AI	97AI	99AI	95AI	99AI	IA66	98AI	98AI	1A66	99AI
KIND OF	., Ш		Si ₃ N ₄	Si ₃ N,	AIN	AIN	Si-AI-0-N	Si-Al-0-N	SiC	SiC	Al,03	Al ₂ 0 ₃	Sink	Si ₃ N ₄	Si ₃ N ₄	N.i.S	Si ₃ N,	Si ₃ N,	Si ₃ N,	SigN	Si ₃ N ₄	Si ₃ N,	Si ₃ N,	N.iS	Si ₃ N ₄	Si ₃ N	Si ₃ N ₄				L	
	SAMPLE No.		EXAMPLE 1	EXAMPLE 2			EXAMPLE 5	EXAMPLE 6	EXAMPLE 7	EXAMPLE 8	EXAMPLE 9	EXAMPLE 10	EXAMPLE 11	EXAMPLE 12	EXAMPLE 13	EXAMPLE 14	EXAMPLE 15	EXAMPLE 16	EXAMPLE 17	EXAMPLE 18	EXAMPLE 19	EXAMPLE 20	EXAMPLE 21	EXAMPLE 22	EXAMPLE 23	EXAMPLE 24	EXAMPLE 25	EXAMPLE 26	EXAMPLE 27	EXAMPLE 28	EXAMPLE 29	EXAMPLE 30

TABLE 1]

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VOID	RATIO	(%)	0.1	6.0	6.0	1.8	4.8	1.6	0.8	1.8	0.3	1.6	1	1.9	0	1.8	0	0.5	1.8	1.5	4.6	0.1	2.3	2	0	-	0.2	6.0	0	1.2	2.4	2
JOINING	STRENGH	(N∕20mm□)	60.1	51.6	57.9	54.3	50.9	57.6	58.1	55.8	59.6	54.1	58.3	56.6	65.7	56.9	63.8	59.1	57	58.6	51.3	62.8	53.6	55.5	64	60.3	59.1	58.3	62.5	58.4	54.9	53.4
1ENT	TEMPE- RATURE	(၁)	615	630	630	630	630	630	620	580	615	615	615	615	280	280	009	290	009	605	605	610	610	605	615	630	630	620	580	615	620	625
JOINING TREATMENT	DEGREE OF VACUUM	(Pa)	10-2	10-2	10-2	10-2	10-2	10-2	10_2	10-2	10_5	10-2	10-2	10_5	10-2	10_5	10-2	10-2	10-2	10-2	10_5	10_2	10_5	10_5	10_2	10_5	10-2	10_5	10_5	10-2	10-2	10-2
NINIOC	PRESSING LOAD	(MPa)	1.5	0.3	0.5	1	0.2	0.5	-	0.5	1	0.5	0.5	0.5	0.5	0.2	1,5	1	0.5	0.2	0.2	1	0.5	1.5	2	0.5	0.5	1	1	0.5	0.2	0.5
SURFACE STRATE	THICKNESS	(m m)	0.2	0.3	8.0	8.0	0.5	0.3	0.5	0.1	0.3	8.0	0.3	0.5	0.3	9.0	0.3	8.0	0.5	0.2	0.2	0.3	0.1	9.0	9.0	0.3	0.5	8.0	0.3	9.0	0.5	0.3
AI ALLOY FILM ON SURFACE OF CERAMIC SUBSTRATE	COMPOSITION	(at%)	4Ce-Al	5Dy-Al	3Y-AI	5Nd-Al	1Nd-Al	3Gd-0.5Y-AI	2Ce-Er-Al	3G4-0.5Y-AI	3Nd-La-Al	3Nd-La-A	3Y-AI	3Nd-AI	3Y-AI	5Gd-Al	3Y-AI	2Sr-AI	2Ce-Al	2Dy-Al	4Th-AI	3Y-AI	5Tb-Al	5Er-Al	5Dy-Al	3Y-AI	3Ce-1.5Sr-Al	3La-2Gd-AI	3.5Er-0.5Y-AI	2Sr-2Dy-Al	2Sm-1Nd-Al	3Y-AI
(CIRCUIT LAYER)	TOTAL THICKNESS	(mm)	0.3	0.2	0.3	0.5	0.3	0.2	0.15	0.5	0.3	0.5	0.2	0.2	0.15	0.2	0.5	0.2	0.15	0.5	0.1	0.3	0.5	0.4	0.2	0.3	0.2	0.3	0.5	0.5	0.15	0.2
) MEMBER	MPOSITION OF -Si BRAZING	MATERIAL (MASS%)	7.5Si-Al	7.5Si-AI	6Si-Al	6Si-Al	6Si-Al	6Si-Al	7.5Si-AI	12Si-Al	15Si-AI	7.5Si-Al	15Si – Al	15Si Al	12SiAl	12Si-Al	10Si Al	10Si Al	10Si – Al	10Si-Al	7.5Si-Al	7.5Si-AI	7.5Si-AI	7.5Si—AI	7.5Si-Al	6Si-Al	6Si-Al	15SiAI	12SiAl	7.5Si — Al	7.5SiAI	15Si-Al
STRUCTURE OF CLAI	E E	(MASS%)	98AI	95AI	99AI	98Ai	97AI	95AI	95AI	97AI	95AI	98AI	99AI	97AI	1966	98AI	99AI	97AI	99AI	95AI	99AI	99AI	98AI	99AI	95AI	99AI	95AI	95AI	97AI	98AI	95AI	99AI
KIND OF	., Ш		S _{i3} N ₄	SisN	Si _o V,	Si ₃ N ₄	Si ₃ N _¢	Si ₃ N ₄	Si ₃ N ₄	Ain	AIN	AIN	NE	AIN	AIN	NIA	NIA	AIN				Sil										
	SAMPLE No.		EXAMPLE 31	EXAMPLE 32	EXAMPLE 33	EXAMPLE 34	EXAMPLE 35	EXAMPLE 36	EXAMPLE 37	EXAMPLE 38	EXAMPLE 39	EXAMPLE 40	EXAMPLE 41	EXAMPLE 42	EXAMPLE 43	EXAMPLE 44	EXAMPLE 45	EXAMPLE 46	EXAMPLE 47	EXAMPLE 48	EXAMPLE 49	EXAMPLE 50	EXAMPLE 51	EXAMPLE 52	EXAMPLE 53	EXAMPLE 54	EXAMPLE 55	EXAMPLE 56	EXAMPLE 57	EXAMPLE 58	EXAMPLE 59	EXAMPLE 60

[TABLE 2]

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	KIND OF	STRUCTURE OF CL	AD MEMBER	(CIRCUIT LAYER)	AI ALLOY FILM ON SURFACE OF CERAMIC SUBSTRATE	SURFACE STRATE	NIOL	JOINING TREATMENT	ENT	JOINING	QIOA
SAMPLE No.	CERAMIC SUBSTRATE	T IN	Ö `	TOTAL THICKNESS	COMPOSITION	THICKNESS PRESSING DEGREE OF LOAD VACUUM	PRESSING LOAD	DEGREE OF VACUUM	TEMPE- RATURE	STRENGH	AREA RATIO
		(MASS%)	MATERIAL (MASS%)	(mm)	(at%)	(m m)	(MPa)	(Pa)	္မွ	(N/20mm[])	(%)
EXAMPLE 61	Si-Al-0-N	97AI	15Si-AI	0.2	3Nd-AI	0.5	0.2	10-2	620	50.9	3.8
EXAMPLE 62	EXAMPLE 62 SI-AI-0-N	99AI	12Si-AI	0.15	3Y-AI	0.3	1.5	10-2	580	61.6	0
EXAMPLE 63		98AI	12Si-Al	0.2	5Gd-Al	9.0	1.5	10-2	580	59.2	0.2
EXAMPLE 64	Si-Al-0-N	99AI	10Si AI	0.5	3Y-AI	0.3	2	10-2	009	63.8	0
EXAMPLE 65	Si-AI-0-N	97Ai	10Si-Al	0.2	2Sr-Al	8.0	0.5	10-2	605	52.6	1.8
EXAMPLE 66	Si-AI-0-N	99AI	10Si-Al	0.15	2Ce-Al	0.5	_	10-2	610	55.2	6.0
EXAMPLE 67	Si-Al-0-N	95AI	10Si-Al	0.5	2Dy-Ai	0.2	0.5	10_5	610	55.5	4.1
EXAMPLE 68	Si-AI-0-N	99AI	7.5Si-Al	0.1	4Th-AI	0.2	0.2	10-2	610	46.4	8.2
EXAMPLE 69	Si-AI-0-N	99AI	7.5Si-Al	0.3	3Y-AI	0.3	1	10-2	615	59.9	0.3
EXAMPLE 70	Si-AI-0-N	98AI	7.5Si-AI	0.5	5Tb-AI	0.1	0.2	10-2	620	51.1	2.6
EXAMPLE 71	Si-AI-0-N	99AI	7.5Si-Al	0.4	5Er-Al	9'0	0.5	10-2	630	54.3	1.5
EXAMPLE 72	Si-Al-0-N	95AI	7.5Si-Al	0.5	5Dy-Ai	8.0	1	10-2	620	52.8	4.2
EXAMPLE 73	EXAMPLE 73 Si-AI-0-N	99AI	6Si-Al	0.3	3Y-AI	6.0	1.5	10-2	630	57.8	6.0
EXAMPLE 74	EXAMPLE 74 Si-AI-0-N	95AI	6Si-Al	0.2	3Tb-0.5Y-AI	8'0	0.2	10-2	630	50.3	4.5
EXAMPLE 75			15Si-Ał	0.3	2.5Dy-2Y-AI	0.3	0.5	10-2	620	54.9	2.3
EXAMPLE 76		97AI	12SiAI	0.5	3.5Th-1Ce-Al	9.0	1	10-2	280	59.6	9.4
EXAMPLE 77			7.5Si-Al	0.5	3Y-2Gd-AI	8.0	0.2	10-2	615	48.6	6.4
EXAMPLE 78	Si-AI-0-N	95AI	7.5Si-Al	0.15	2.5Nd-2Th-AI	0.2	-	10-2	620	53.2	4.8
EXAMPLE 79	SiC	99AI	15Si-Al	0.2	3Y-AI	0.3	0.5	10-2	615	51.2	0.5
EXAMPLE 80	Sic	97AI	15Si-Al	0.2	3Nd-AI	0.5	0.2	10-2	610	48.6	6.0
EXAMPLE 81	SiC	99AI	12Si-Al	0.15	3YAI	0.3	1.5	10-2	580	57.8	0
EXAMPLE 82	SiC	98AI	12Si-AI	0.2	5Gd-Al	9.0	0.2	10-2	009	53.5	0.3
EXAMPLE 83	SiC	99AI	10Si-Al	0.5	3Y-AI	0.3	-	10-2	009	56.7	0
EXAMPLE 84	SiC	97AI	10SiAl	0.2	2Sr-Al	8.0	-	10-2	610	52.6	0.2
EXAMPLE 85	SiC	1A66	10Si-Al	0.15	2Ce-Al	0.5	0.2	10-2	610	47.8	1.6
EXAMPLE 86	SiC	95AI	10Si-Al	0.5	2Dy-Al	0.2	0.5	10-2	009	49.8	1.2
EXAMPLE 87	SiC	99AI	7.5Si-AI	0.1	4Th-Al	0.2	0.2	10-2	615	41.9	4.8
EXAMPLE 88	SiC	99AI	7.5Si — AI	0.3	3Y-AI	0.3	2	10-2	615	55.9	0
	SiC	98AI	7.5Si—Al	0.5	5Tb-Ai	0.1	0.5	10_5	620	43.6	2.1
EXAMPLE 90	SiC	99AI	7.5Si-AI	0.4	5Er-Al	9.0	2.5	10-2	610	56.1	0

[TABLE 4]											
	KIND OF	STRUCTURE OF CI	AD MEMBER	(CIRCUIT LAYER)	AI ALLOY FILM ON SURFACE OF CERAMIC SUBSTRATE	SURFACE 3STRATE	JOININ	JOINING TREATMENT	ENT	JOINING	VOID
SAMPLE No.		AI CONTENT IN CIRCUIT LAYER	COMPOSITION OF AI-SI BRAZING	TOTAL THICKNESS	COMPOSITION	THICKNESS		PRESSING DEGREE OF LOAD VACUUM	TEMPE- RATURE	STRENGH	RATIO
		(MASS%)	MATERIAL (MASS%)	(mm)	(at%)	(m m)	(MPa)	(Pa)	(°C)	(N∕20mm□)	(%)
EXAMPLE 91	SiC	95AI	7.5Si-Al	0.2	5Dy-Al	0.8	1	10-2	615	44	2.5
EXAMPLE 92	SiC	1A66	6Si-Al	0.3	3Y-Al	0.3	0.5	10-5	630	51.3	0
EXAMPLE 93	SiC	95AI	6Si-Al	0.2	3Tb-1.5Er-Al	0.8	0.5	10-2	630	48.7	0.4
EXAMPLE 94	SiC	95AI	15Si-Al	0.3	3La-0.5Sm-Al	0.8	0.2	10_5	620	43.5	2.5
EXAMPLE 95	SiC	97AI	12Si-AI	0.5	4Sm-0.5Y-AI	0.5	0.2	10-2	280	42.6	3.2
EXAMPLE 96	SiC	98AI	7.5Si-Al	0.5	2.5Y-1Sr-Al	0.5	-	10-2	615	49.8	0.7
EXAMPLE 97	SiC	95AI	7.5Si—Al	0.15	2.5Y-2Nd-AI	0.2	1	10-2	615	42.4	3.3
EXAMPLE 98		IA66	15Si-Al	0.2	3Y-AI	0.3	0.5	10-2	615	8.09	0.2
EXAMPLE 99	Al ₂ 0 ₃	97AI	15Si-Al	0.2	3Nd-Al	0.5	1	10-2	. 009	64.5	0.1
EXAMPLE 100	Al ₂ 0 ₃	1A66	12Si-Al	0.15	3Y-AI	0.3	1.5	10-2	580	99	0
EXAMPLE 101		188	12Si-Al	0.2	5Gd-Al	9.0	0.5	10-2	580	61.2	0.5
EXAMPLE 102	·	1A66	10Si-Al	0.5	3Y-AI	0.3	2	10-2	595	65.8	0
EXAMPLE 103		97AI	10SiAl	0.2	2Sr-Al	0.8	-	10_2	900	60.5	2.5
EXAMPLE 104		1A66	10Si-Al	0.15	2Ce-Al	0.5	0.2	10-2	610	61.8	9
EXAMPLE 105		95AI	10Si-Al	0.5	2Dy-Al	0.2	0.5	10-2	900	60.4	4.2
EXAMPLE 106		1A66	7.5Si-AI	0.1	4Th-Al	0.2	0.5	10-2	615	58.8	2.9
EXAMPLE 107		99AI	7.5Si-AI	0.3	3Y-AI	0.3	-	10-2	610	64.2	0.1
EXAMPLE 108		98AI	7.5Si-Al	0.5	5Tb-Al	0.1	0.5	10-2	610	60.7	3.6
EXAMPLE 109	Al ₂ 0 ₃	99AI	7.5SiAl	0.4	5Er-Al	9.0	-	10-2	610	61.3	1.9
EXAMPLE 110	L	95AI	7.5Si-Al	0.2	5Dy-Al	0.8	1.5	10-2	615	64.8	0.4
EXAMPLE 111	Al ₂ 0 ₃	1 9 881	6Si-Al	0.3	3Y-Al	0.3	1.5	10-2	620	62.1	0.5
EXAMPLE 112		95AI	6Si-Al	0.2	4Gd-0.5Y-Al	0.2	-	10-2	620	61.5	3
EXAMPLE 113		95AI	15Si-Al	0.3	4Nd-0.5Sm-Al	0.8	-	10-2	620	63.8	0.4
EXAMPLE 114		97AI	12Si-Al	0.5	3.5Er-0.5Y-AI	0.5	2	10-2	580	63.6	0
EXAMPLE 115		98AI	7.5Si-Al	0.5	3Gd-0.5Y-AI	9.0	0.2	10-2	615	63.6	2.1
EXAMPLE 116	Al ₂ 0 ₃	95AI	7.5Si-Al	0.15	2Ce-Er-Al	0.2	0.2	10-2	620	59.7	3.1

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	STRUCTURE OF CLAD	J. J. P. J.	MEMBER (CIR	CUIT LAYER)	AI ALLOY FILM ON SURFACE OF CERAMIC SUBSTRATE	SURFACE 3STRATE	JOININ	JOINING TREATMENT	ENT	JOINING	VOID
YER IN		COMP AI-S	COMPOSITION OF AI-SI BRAZING	TOTAL THICKNESS	COMPOSITION	THICKNESS	PRESSING DEGREE OF LOAD VACUUM	DEGREE OF VACUUM	TEMPE- RATURE	STRENGH	RATIO
(MASS%) MATER		MATE	MATERIAL (MASS%)	(mm)	(at%)	(m m)	(MPa)	(Pa)	(၃)	(N/20mm□)	(%)
Si₃N₄ 98Al 1		-	15Si-Ai	0.2	100A	6.0	8.0	10-2	650	30.2	28.1
C.EXAMPLE 2 Si ₃ N ₄ 97AI 1		-	18Si-Al	0.4	4Gd-AI	0.1	-	10-2	009	36.3	18.2
C.EXAMPLE 3 AIN 98AI 1			10Si-Al	0.5	4Y-1Ce-AI	1.1	9.0	10-2	590	33.9	13.2
C.EXAMPLE 4 SI — AI — 0 — N 97AI	97AI		5Si-Al	0.3	4Nd-AI	0.2	9.0	10-2	009	29.4	20.5
96AI		7.5	7.5Si-Al	0.5	4Y-AI	0.3	0.5	10-2	570	10.5	61.7
C.EXAMPLE 6 Al ₂ 0 ₃ 98Al 10		2	10Si-Al	0.3	3Tb-Al	0.5	0.1	10-2	630	24.6	55.1
AIN 97AI 7.5		7.5	7.5Si-Al	0.5	10Y-AI	0.5	0.5	10-2	009	38.3	15.8
C.EXAMPLE 8 Si ₃ N ₄ 99AI 10S		10S	10Si-Al	0.3	10Y-AI	0.5	0.5	10-2	009	28.4	22.5
C.EXAMPLE 9 Si ₃ N ₄ 99AI 10S		10S	10Si-Al	0.3	10Sc-Al	0.5	0.5	10-2	009	24.6	26.4
C.EXAMPLE 10 Si ₃ N ₄ 99Ai 10S		108	10SiAl	0.3	10La-Al	0.5	0.5	10-2	009	27.2	20
AIN 99AI 10S		10S	10Si – Al	0.3	10Ce-Al	0.5	0.5	10-2	009	33.6	15.8
C.EXAMPLE 12 AIN 99AI 10S		10S	10Si Al	0.3	10Nd-Al	0.5	0.5	10-2	009	30.2	16.7
C.EXAMPLE 13 AIN 98AI 10S		108	10Si-Al	0.3	10Sm-Al	0.5	0.5	10-2	009	28.7	21.5
C.EXAMPLE 14 Al ₂ 0 ₃ 99Al 10S		108	IOSi-AI	0.3	10Gd-Al	0.5	0.5	10-2	. 009	33	17
1A99		108	10Si-Al	0.3	10Tb-Al	0.5	0.5	10-2	009	31.2	20.1
C.EXAMPLE 16 Al ₂ 0 ₃ 99Al 105		20	10Si AI	0.3	10Dy-Al	0.5	0.5	10-2	009	37.3	15.8
C.EXAMPLE 17 SiC 99AI 10S		108	10Si-Al	0.3	10Er-Al	0.5	0.5	10-2	009	31.3	15.2
C.EXAMPLE 18 SiG 99AI 10		10	10Si-Al	0.3	10Th-Ai	0.5	0.5	10-2	009	32.5	15.1
C.EXAMPLE 19 Si—AI—0—N 99AI 10		2	10Si – Al	0.3	10Sr-AI	0.5	0.5	10-2	909	29.4	17.5
C.EXAMPLE 20 Si ₃ N ₄ 99AI 128		125	12Si-Al	0.3	3Y-AI	1.5	0.5	10-2	580	30.4	15.9
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NOTE: C.EXAMPLE denotes COMPARATIVE EXAMPLE.

	NOID	AREA	(% (%	L	65.2	30.4	33.2	21.3	46.7	22.6	15.7	64.5	20.6	74.3	23.2	18.2	15.9	13.6	16.8	16.7	15.5	18	19.6	15.1	23	35.6	17.4	18.5
	SNINICI	STRENGH	(N∕20mm□)	10.4	11.6	28.7	25.9	38.7	21.6	33.4	28.9	12.1	34.2	9.6	28.6	34.5	28.2	35.6	31.2	31.2	36.6	33.4	30.8	33.4	19.5	20.5	34.1	32.5
	ENT	TEMPE- RATURE	(၃)	580	570	640	640	580	280	580	009	009	009	009	570	640	640	580	580	900	009	909	909	009	570	640	640	640
	JOINING TREATMENT	PRESSING DEGREE OF LOAD VACUUM	(Pa)	10-2	10-2	10-2	10-2	10-2	10_2	10-2	10_5	10-2	10-2	10-2	10-2	10-2	10-2	10-2	10-2	10_5	10_5	10-2	10_5	10-2	10-1	10-2	10-2	10-2
	INIOr		(MPa)	0.1	0.5	0.5	0.5	0.8	0.5	0.5	0.5	0.1	0.5	0.1	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
	SURFACE 3STRATE	THICKNESS	(m m)	0.3	0.3	0.3	0.3	0.3	0.3	0.3	1.5	0.3	1.5	0.3	0.3	0.3	0.3	0.3	0.3	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
	AI ALLOY FILM ON SURFACE OF CERAMIC SUBSTRATE	COMPOSITION	(at%)	3Y-Ai	3Y-AI	3Y-Ai	3Y-Al	100Al	3Y-AI	3Y-AI	3N4-AI	3Nd-Al	3G4-AI	3G4-AI	3Er-Al	3Ce-At	3Nd-AI	4G4-AI	4Sc-Al	5Gd-3Y-AI	5Ce-3Er-Al	5Gd-3Y-AI	5Nd-3La-Al	5Y-5Er-AI	4Gd-0.5Y-Al	4Nd-0.5Sm-Al	3.5Er-0.5Y-AI	3Gd-0.5Y-Al
	(CIRCUIT LAYER)	TOTAL THICKNESS	(mm)	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3
	LAD MEMBER	COMPOSITION OF AI-SI BRAZING	MATERIAL (MASS%)	12Si Al	12SiAI	6Si-Al	12Si-Al	12Si-Al	18Si-Al	5Si-Al	10Si-Al	10Si-Al	10Si-Al	10Si-Al	12SiAl	6Si-Al	12Si-Al	18SiAI	5Si-Al	10Si-Al	10SiAl	10Si-Al	10Si-AI	10Si-Al	12Si-Al	6Si-Al	12Si – Al	10Si-Al
	STRUCTURE OF C	E E	= 	99AI	99AI	99AI	99AI	98AI	99AI	99AI	99AI	99Al	99Al	99AI	99AI	99AI	99AI	99AI	99AI	99AI	99AI	99AI	99AI	99AI	99AI	99AI	99AI	99AI
	KIND OF	CERAMIC SUBSTRATE		Si ₃ N ₄	Si ₃ N ₄	Si ₃ N ₄	AIN	Ν̈́	Si ₃ N ₄	Si-Al-0-N	Si-Ai-1-N	Si ₃ N ₄	Si ₃ N¢	SiC	Sic	Si ₃ N ₄	Si ₃ N ₄	NIA	Al ₂ 0 ₃	Si ₃ N ₄	Si-Al-0-N	AIN	Al ₂ 0 ₃	SiC	Si ₃ N ₄	Al ₂ 0 ₃	AIN	Ain
[TABLE 6]		SAMPLE No.		C.EXAMPLE 21	C.EXAMPLE 22	C.EXAMPLE 23	C.EXAMPLE 24	C.EXAMPLE 25	C.EXAMPLE 26		_	C.EXAMPLE 29	C.EXAMPLE 30	C.EXAMPLE 31	C.EXAMPLE 32	C.EXAMPLE 33	C.EXAMPLE 34	C.EXAMPLE 35	C.EXAMPLE 36		_	C.EXAMPLE 39	C.EXAMPLE 40	C:EXAMPLE 41	C.EXAMPLE 42	C.EXAMPLE 43	C.EXAMPLE 44	C.EXAMPLE 45

NOTE : C.EXAMPLE denotes COMPARATIVE EXAMPLE.

As is apparent from the results shown in Tables 1 to 6, according to the ceramic circuit boards of the examples each prepared by forming an Al alloy film having a predetermined thickness on the surface of the ceramic substrate, even when the thickness of the Al alloy film is small to be less than 1 µm, the void area ratio was smaller than that of the comparative examples. This result showed that the diffusion and the ejection (the hillock phenomenon) of Al elements on the joint surface during joining by heating were effectively suppressed.

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Therefore, it was confirmed that the generation of voids in the joint surface could be effectively prevented and the joint strength was drastically increased and thus improved. Furthermore, since the thickness of the Al alloy film could be decreased to be less than 1 µm, the time required for depositing the Al alloy film by vapor deposition or the like could be reduced and the joining operation could be simplified. Therefore, it became clear that the joint assembly of the circuit board could be simplified to reduce the production cost drastically.

On the other hand, according to the ceramic circuit board of Comparative Example 1 prepared by forming an AI metal layer on the surface of the ceramic substrate in advance, the diffusion of AI elements during joining by heating was significant and the ejection (the hillock phenomenon) of AI elements on the joint surface was not suppressed. It was reconfirmed that the joint strength was also drastically decreased in proportion to the sharp increase in the void area ratio.

In addition, as shown in Comparative Examples 2 to 7, the results showed that when the composition of the Al alloy film (Comparative Examples 1 and 7), the joint temperature (Comparative Examples 1 and 5), the composition of Al-Si brazing material (Comparative Examples 2 and 4), the thickness of the Al alloy film (Comparative Example 3), the pressure during joining (Comparative Example 6), or the like were out of the preferred range specified in the present invention, the joint

strength of the circuit layer and the void area property were decreased.

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Fig. 2 is a cross-sectional view showing an example of the structure of a power module including the ceramic circuit board according to an embodiment of the present invention. Namely, on the surface of an Al circuit plate 2 of a ceramic circuit board 1 disposed in a power module 10 of this embodiment, a semiconductor chip (semiconductor element) 11 including an IGBT (insulated gate bipolar transistor) serving as a power device is fixed with solder 12.

The Al circuit plate 2 is connected to an electrode terminal (not shown in the figure) for a collector and supplies the semiconductor chip 11 with a collector voltage. Both ends of a bonding wire 13 composed of a fine wire of a metal such as Al or Au are bonded to a gate electrode 14 on the semiconductor chip 11 and a metal film 15 on a ceramic substrate 6, respectively, by using ultrasonic welding. Since the metal film 15 is connected to an electrode terminal (not shown in the figure) for a gate, the bonding wire 13 is electrically connected to the electrode terminal for the gate. Thus, a gate voltage is supplied from the electrode terminal for the gate through the bonding wire 13.

Further, both ends of a bonding wire 16 are bonded to an emitter electrode 17 on the semiconductor chip 11 and a metal film 18 on the ceramic substrate 6, respectively, by using ultrasonic welding. Since an electrode terminal 19 for an emitter is bonded on the metal film 18 with solder 20, the bonding wire 16 is electrically connected to the electrode terminal 19 for the emitter. Thus, an emitter voltage is supplied from the electrode terminal 19 for the emitter through the bonding wire 16.

The bottom face of the ceramic substrate 6 is joined on a metal substrate (heat sink) 24 with a metal film 22 and solder 26 that are provided therebetween. An outer shell case 28 composed of a plastic material or the like and the metal substrate 24

constitute a package 29. The semiconductor chip 11, the ceramic substrate 6, the Al circuit layer 2, the metal films 15 and 18, the bonding wires 13 and 16, and a part of the electrode terminal 19 for the emitter are sealed in the package 29 to constitute the single power module 10. The metal substrate 24 can be formed as a component also serving as a heat sink, but radiation fins (heat sink) may be separately provided in addition to the metal substrate 24. Heat generated from the semiconductor chip 11 is dissipated to the bottom face side of the semiconductor chip 11 through the metal substrate 24, thereby cooling the semiconductor chip 11. Thus, the operation and the function of the semiconductor chip 11 are satisfactorily maintained.

According to the power module of the embodiment having the above-described structure, the generation of voids in the joint interface of the ceramic substrate can be effectively suppressed, and thus the joint strength of the metal member serving as the circuit layer can be increased. Consequently, a power module in which the heat resistance cycle characteristics can be drastically improved can be obtained and satisfactory reliability can be ensured.

Industrial Applicability

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According to the ceramic circuit board, the method for producing the same, and the power module of the present invention, since an Al alloy film having a predetermined thickness is formed on the surface of a ceramic substrate, even when the thickness of this Al alloy film is small to be less than 1 µm, the diffusion and the ejection (the hillock phenomenon) of Al elements on the joint surface during joining by heating can be effectively suppressed, the generation of voids in the joint surface can be effectively prevented, and the joint assembly of the circuit board can be simplified thereby to reduce the production cost drastically.